I claim:

1. A memory device, comprising:

a multiplicity of memory cells for storing data;

comparison units each having an address input and being configured to check whether an address applied to the memory device is associated with a memory cell which cannot be properly written to or read out or is located in a memory cell area containing memory cells which cannot be properly written to or read out; and

wherein, during in a testing phase of the memory device, said comparison units are placed into a testing state different from a state during a normal operation of the memory device.

2. The memory device according to claim 1, wherein said comparison units are configured to compare the address applied to the memory device with reference addresses associated with said comparison units.

3. The memory device according to claim 2, wherein each said comparison unit has associated therewith an individual reference address.

4. The memory device according to claim 2, wherein said comparison units operate in parallel and compare the address applied to the memory device simultaneously with all reference addresses.

5. The memory device according to claim 2, wherein said comparison units are each associated with a respective memory area of the memory device by the reference addresses, and are configured to compare whether the address applied to the memory device is within the memory area respectively associated therewith.

6. The memory device according to claim 2, wherein the addresses of the memory cells which cannot be properly written to or read out or of the memory cell areas containing memory cells which cannot be properly written to or read out are defined as reference addresses.

7. The memory device according to claim 2, wherein test addresses suitable for testing the memory device are defined as reference addresses.

8. The memory device according to claim 7, wherein the test addresses are used during the testing of the memory device.

9. The memory device according to claim 8, wherein the test addresses are specified independently of the reference addresses with which the comparison units normally compare the addresses applied to the memory device.

10. The memory device according to claim 1, wherein the reference addresses can be registered at least partially permanently in the memory device.

11. The memory device according to claim 10, which comprises a plurality of fuses defining the registration of the addresses.

12. The memory device according to claim 1, wherein, during the testing phase of the memory device, only selected comparison units are activated and all other comparison units are deactivated.

13. The memory device according to claim 12, wherein said comparison units are selectively activatable and deactivatable, during the testing of the memory device, independently of whether said comparison units are activated or deactivated in normal operation of the memory device.

14. The memory device according to claim 12, wherein only such a number and such comparison units are activated that at

a maximum one of the activated comparison units can find a correspondence for each address applied to the memory device.

15. The memory device according to claim 12, wherein such a number and such comparison units are activated that the memory areas with which the activated comparison units are associated or can be associated by means of their reference address comprise all memory cells which can be addressed by the addresses applied to the memory device.

16. A method of operating a memory device, which comprises providing a memory device with a multiplicity of memory cells for storing data and a plurality of comparison units according to claim 1, checking, with the comparison units, whether an address applied to the memory device is associated with a memory cell which cannot be properly written to or read out or is located in a memory cell area containing memory cells which cannot be properly written to or read out, and, during a testing of the memory device, placing the comparison units into a state which differs from a state of the comparison units during a normal operation of the memory device.

17. The method according to claim 16, which comprises comparing with the comparison units the address applied to the memory device with reference addresses associated with the comparison units.

18. The method according to claim 17, which comprises operating the comparison units in parallel and comparing, with the comparison units, the address applied to the memory device simultaneously with all reference addresses.

19. The method according claim 17, which comprises associating each of the comparison units with a particular memory area of the memory device by the reference addresses and checking, with comparisons carried out by the comparison units, whether the address applied to the memory device is within the memory area with which the specific comparison unit are associated in each case.

20. The method according to claim 17, which comprises utilizing the addresses of the memory cells which cannot be properly written to or read out or of the memory cell areas containing memory cells which cannot be properly written to or read out as reference addresses.

21. The method according to claim 17, which comprises defining test addresses suitable for testing the memory device as reference addresses.

22. The method according to claim 21, which comprises utilizing the test addresses during the testing of the memory device.

23. The method according to claim 22, which comprises specifying the test addresses independently of the reference addresses with which the comparison units normally compare the addresses applied to the memory device.

24. The method according to claim 16, which comprises registering the reference addresses at least partially permanently in the memory device.

25. The method according to claim 16, which comprises, during the testing of the memory device, activating only selected comparison units and retaining all other comparison units deactivated.

26. The method according to claim 25, which activating only such a number and such comparison units that at a maximum one of the activated comparison units can find a correspondence for each address applied to the memory device.

27. The method according to claim 25, which comprises activating such a number and such comparison units that the memory areas with which the activated comparison units are

associated or can be associated by means of their reference address comprise all memory cells which can be addressed by the addresses applied to the memory device.